Outline

1. The Enabling Technology and Motivation
   • Smart Pixel Architecture and Design

2. Smart Pixel Array Cellular Logic (SPARCL) processor
   • SPARCL IC logic design and its application MPEG video sequence process
   • Diffractive microlens array for smart pixel optical interconnects
   • SPARCL testing and system implementation

3. Smart Pixel Array for Networking (SAPIENT)
   • Smart Pixel IC design for network Add/Drop Multiplexing

4. Translucent Smart Pixel Array (TRANSPAR)
   • Smart Pixel IC design for ring connected gigabit Ethernet

5. Summary
Motivation – Gap between on-chip and off-chip speed

- 0.25µm CMOS technologies allow on-chip clock rates 6 GHz
- opto-electronic devices can operate at data rates exceeding 2 GHz
- difficult to drive circuitry at such high rates on a printed circuit board
  - complex and expensive board layout techniques are required above 400 MHz
  - connector footprints limit the number of signal channels that can be used
Hybrid CMOS/SEED Technology (Lucent Tech)

- SEED devices are flip-chip bonded to standard foundry CMOS circuitry.
- Speed of optical link limited by electronics, not SEEDs (125 fF).
- Lucent has demonstrated:
  - High density SEEDs (> 28,000 /cm²) on high performance CMOS.
  - High speed (1 Gb/s links).
  - Low power (< 1 mW/link @ 155 Mb/s).
Structure of Vertical Cavity Surface-Emitting Laser (VCSEL)
Vertical Cavity Surface Emitting Lasers (VCSELs) on CMOS

- Integrate VCSELs, CMOS and diffractive optic elements
- Ultra-low threshold VCSELs are becoming a reality
  - $I_{\text{th}} = 8.7 \, \mu\text{A}$ in $3 \, \mu\text{m}^2$ structure (Dapkus-USC)
  - $I_{\text{th}} < 200 \, \mu\text{A}$ available for arrays in near future
CMOS/MQW Smart Pixel Architecture

- Vdd = 3V
- Vmod = 11V
- Vdet = 11V
- Vmod = -8V
- Vdet = -8.8V
Optical Bits Transmission and Receiving Mechanism

- A bit of “0” transmitted from chip 1 to chip 2
- \( V_{\text{mod}} \) and \( -V_{\text{mod}} \) bias transmitter at zero
- \( V_{\text{det}} \) and \( -V_{\text{det}} \) bias receiver at transition point
Energy for Optical and Electrical Communications

(Courtesy of AT&T)
Ultimate Limits of Si

Smart Pixel Examples

Comparison of SIMD Architectures with Free Space Optical Interconnects Technology

- Assume the same total number of processors
- 1-D and 2-D nSPARCL outperform SIMD
- SPARCL is best for input-output limited high capacity parallel processing
Smart Pixel ARray Cellular Logic (SPARCL)
Parallel Pipeline SIMD Processing System

- Free space digital optics (FSDO):
  - Pipeline high capacity smart pixel arrays to reduce latency
  - Programmable SIMD parallel data processing

- Demonstrate large chip pinouts with smart pixel arrays
  - The 2 x 2 mm SPARCL chip has 40 electrical I/Os (wire bonds) and 200 optical I/Os (detectors and modulators)

- Applications
  - Image or parallel data processing with cellular logic
  - Parallel optical data packet transfer and header recognition
  - Examples: edge detection, noise filtering, motion estimation, data buffering (serial <-> parallel conversion)
SPARCL as Programmable General Purpose Parallel Processing System

• Mathematical morphological processing
  - basic operations (e.g. dilation, erosion, closing, opening, thinning, skeleton)
  - image feature extraction (e.g. edge detection, shape/size/location verification)
  - image enhancement (e.g. salt and pepper noise removal)
  - parallel pattern recognition (e.g. hit-miss transformation, template matching)
  - Interframe operations (e.g. differencing, motion estimation)

• Parallel numerical computation
  - addition, subtraction, multiplication and division

• Combinatorial logic functions

• Serial-to-parallel or parallel-to-serial data format conversion and buffering
Schematic Design and Layout of Smart Pixel ARray Cellular Logic (SPARCL) Chip

- Each smart pixel contains:
  - one bit dual-rail optical detector + one bit dual-rail optical transmitter
  - three single-bit memories
  - three fundamental binary morphology algebra logic of OR, COMPLEMENT and DILATION
  - complete morphological image processing functions

- 5 x 10 CMOS/MQW smart pixel array
- Standard 0.8 \( \mu \text{m} \) HP CMOS process through MOSIS
- MQW foundry service from Bell Labs/Lucent Technologies
SPARCL Difference Operation

\[ B_0 \cup B_1 = \bar{B}_0 \cup \bar{B}_1 \]

\[ D = \bar{B}_1 \cup B_0 \]
MPEG Sequence Prediction Structure

- I: Intra-coded frame
- P: Predictive-coded frame
- B: Bi-directional predictive-coded frame

- Expected high temporal redundancy between frames

sequence 30 frames/sec
Transmission of Compressed Digital Video Sequence

Transmitter Site

- 5 x 10 data block
- Search for best matched block w/ SPARCL

Receiver Site

- Previous frame
- motion compensated image
- JPEG decoder
- Motion vectors
- Difference image
- Recovered current frame

• Search for best matched block in real time requires 3 GOPS
• Instead of xmitting current frame and waste bandwidth, motion vectors and difference image are xmted
• Block oriented SPARCL architecture performs search for the best match block efficiently
SPARCL Digital Video Motion Estimation

1. Search the best matching block by scrolling the search area in the previous frame through the 1st chip.

2. Data block $B_1$ from the current frame waits in the local memory of the 2nd chip is correlated with $B_0$ and produces difference image $D = B_0 \cup B_1$.

3. Chip 3 collects the results and unloads to the host computer.
Hybrid CMOS/SEED SPARCL Chip

- AT&T/ARPA CO-OP Hybrid SEED Program
- 200 MQW diodes (SEEDs) are flip-chip bonded to 0.8 µm CMOS circuitry providing free-space optical data I/O
- Chip contains 5 x 10 array of smart pixels
  - 182 transistors per pixel
  - 13k total on chip

- MQW foundry service from Bell Labs/Lucent Technologie
Diffractive Micro-Lens Array

• Diffractive microlens array provide compact, scalable imaging for SPAs
• Honeywell fabrication through CO-OP
• 10 x 20 array
• 62.5 x 125 \( \mu \text{m} \) aperture
• \( f/7 \) (1 mm focal length)
  – 8 phase level
  – 95% efficiency
• \( f/3 \) (300 \( \mu \text{m} \) focal length)
  – hybrid number of phase levels
  – 83 % efficiency
Idea - Hybrid Phase Level Microlens

- Representing kinoform microlens profile with different phase levels

- Continuous phase surface

- Eight phase level surface

- Four phase level surface

- Hybrid phase level surface

- By hybridizing small feature inserted phase level with base phase levels, higher diffraction efficiency at higher N.A. can be achieved.
Diffraction Efficiency v.s. Numerical Aperture

- The diffraction efficiency ($\eta$) of a standard diffractive microlens increases with the number of fabrication phase levels ($L$)
  
  \[ \eta = \text{sinc}^2(1/L) \]

- The numerical aperture (N.A.) of a diffractive microlens is limited by the fabrication linewidth ($w$) and phase level ($L$)
  
  \[ \text{N.A.} = \frac{\lambda}{wL} \]

- To achieve higher N.A., fewer phase levels can be used at the sacrifice of diffraction efficiency

- However, degradation of diffraction efficiency is significant for fewer phase level ($L=2,4$) microlenses.

- Need method to improve N.A. and $\eta$ simultaneously
Analysis of Two Hybrid Phase Level Microlens Properties

- Conventional microlens with $L_0$ phases: $\eta = \left( \frac{\sin(\pi/L_0)}{\pi/L_0} \right)^2$

  - minimum linewidth $w_0 = \frac{r_p}{L_0} \left( \sqrt{N_0} - \sqrt{N_0 - 1} \right) \approx \frac{r_p}{2L_0 \sqrt{N_0}}$

  where $r_p$ is period of radius and there are total of $N_0$ periods in the aperture

- Two hybrid phase microlens
  - base phase level $= L_0$ and inserted phase level $= L_1$ ($L_1 > L_0$)

  - In the inserted phase region,
    minimum linewidth $w_1 = \frac{r_p}{2L_1 \sqrt{N_1}}$

  - Since $w_1 = w_0$, so $\sqrt{N_1} = \frac{L_0}{L_1}$

  - let $\alpha$ be the radius ratio of phase $L_1$ over $L_0$ then $\alpha = \frac{\sqrt{N_1} r_p}{R} = \frac{\sqrt{N_1} r_p}{\sqrt{N_0} r_p} = \frac{L_0}{L_1}$

  - the hybrid efficiency is then $\eta = \alpha^2 \eta_1 + (1 - \alpha^2) \eta_0$

  - the hybrid efficiency is linear combination of pure efficiencies weighted by the fraction of occupying area, and depends only on number of phase levels $L_1$ and $L_0$ !!!
Optimization of Two Hybrid Phase Levels Microlens

(a) Base phase level = 2

- Standard binary microlens $\eta = 40.5\%$
- Optimized hybrid efficiency = 52.9% with inserted hybrid phase level = 3

(b) Base phase level = 4

- Standard binary microlens $\eta = 81.1\%$
- Optimized hybrid efficiency = 85.6% with inserted hybrid phase level = 6
Generalized Multiple Hybrid Phase Level Microlens

- Optimize numerical aperture and diffraction efficiency with multiple numbers of phase levels $L_0, L_1, L_2, ..., L_{n-1}$ available from fabrication process
- Starting from the center of the aperture with tightest quantization phase level $L_{n-1}$. As soon as radius increases and the quantization phase width reaches min linewidth $w$, it changes to the next lower phase level $L_{n-2}$. The steps continue until the whole aperture is coded.
- The hybrid microlens result N.A. $= \frac{\lambda}{(w L_0 )}$
- Let radius ratios $\alpha_1 = L_0 / L_1$, $\alpha_2 = L_0 / L_2$, $\ldots$, $\alpha_{n-1} = L_0 / L_{n-1}$ then the result hybrid diffraction efficiency is the linear combination of pure efficiencies $\eta_i$ weighted by the fraction of occupying area of the aperture
  \[ \eta = \alpha_{n-1}^2 \eta_{n-1} + (\alpha_{n-2}^2 - \alpha_{n-1}^2) \eta_{n-2} + \cdots + (\alpha_1^2 - \alpha_2^2) \eta_1 + (1 - \alpha_1^2) \eta_0 \]
  \[ = \sum_{i=0}^{n-1} (\alpha_i^2 - \alpha_{i+1}^2) \eta_i \]
  where $\alpha_0 = 1$ and $\alpha_n = 0$
- Example with 2, 4, and 8 multiple phase levels
Relation of Hybrid Phase Level and Area

- The occupying area radius \( r \) of each phase level is inversely proportional to the number of phase levels \( L \)

\[
\frac{r_8}{r_4} = \frac{4}{8} = \frac{1}{2}
\]

\[
r_8 : r_4 : r_2 = 1 : 2 : 4
\]
Design and Fabrication of Diffractive Microlens Array

- 10x20 diffractive micro-lenslets for spot array generation
- Adaptive hybrid number of phase levels to achieve small F/#, high N.A., improved efficiency microlens
- Square aperture: 62.5 x 62.5 - 625 x 625 µm²; rectangular aperture 125 x 62.5 µm²
- Fabrication linewidth 1.5 µm
- F/# 1.74 - 10
- Focal length 0.3 - 3 mm
- Efficiency 43% - 94%

<table>
<thead>
<tr>
<th>Lenslet Array</th>
<th>F/#</th>
<th>focal length (µm)</th>
<th>lenslet aperture (µm²)</th>
<th>phase levels</th>
<th>min feature (µm)</th>
<th>diffraction efficiency</th>
<th>array size</th>
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<tbody>
<tr>
<td>1</td>
<td>1.7</td>
<td>491</td>
<td>200 x 200</td>
<td>8/4/2</td>
<td>1.41</td>
<td>48.39%</td>
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<tr>
<td>2</td>
<td>1.7</td>
<td>3070</td>
<td>625 x 625</td>
<td>8/4/2</td>
<td>1.41</td>
<td>48.12%</td>
<td>2 x 2</td>
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<tr>
<td>3</td>
<td>10</td>
<td>884</td>
<td>62.5 x 62.5</td>
<td>8</td>
<td>2.15</td>
<td>94.57%</td>
<td>10 x 20</td>
</tr>
<tr>
<td>4</td>
<td>3.53</td>
<td>493</td>
<td>125 x 62.5</td>
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<td>0.75</td>
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<td>10 x 20</td>
</tr>
<tr>
<td>5</td>
<td>7.06</td>
<td>986.5</td>
<td>125 x 62.5</td>
<td>8</td>
<td>1.53</td>
<td>94.57%</td>
<td>10 x 20</td>
</tr>
<tr>
<td>6</td>
<td>3.53</td>
<td>493</td>
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<td>7</td>
<td>7.06</td>
<td>624</td>
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<td>8</td>
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<td>94.65%</td>
<td>10 x 20</td>
</tr>
<tr>
<td>8</td>
<td>3.53</td>
<td>312</td>
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<td>1.5</td>
<td>79.94%</td>
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<tr>
<td>9</td>
<td>3.53</td>
<td>312</td>
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<td>8/4</td>
<td>1.5</td>
<td>84.13%</td>
<td>10 x 20</td>
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</table>

Focal length profile and adaptive feature
Optomechanical Interface for SPARCL Network

FIFO/SPARCL BOARD

20 MHz

TEC

LDD

TEC

LDD

TEC

TEC

SPARCL/PCB

computer

clock

100kHz

laser diode module

DOE

PM

λ/4

λ/4

PBS

to next stage

from previous stage

computer interface and chip housing

baseplate optics

laser diode modules

SPARCL baseplate setup

laser diode modules
Spot Diagram Analysis

<table>
<thead>
<tr>
<th>FULL FIELD</th>
<th>FULL FIELD</th>
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<tr>
<td>1.93 deg</td>
<td>0.7 FIELD</td>
</tr>
<tr>
<td></td>
<td>0.531 deg</td>
</tr>
<tr>
<td></td>
<td>0.7 FIELD</td>
</tr>
<tr>
<td></td>
<td>0.006256</td>
</tr>
<tr>
<td></td>
<td>0.003502</td>
</tr>
<tr>
<td>ON-AXIS</td>
<td>0 deg</td>
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<tr>
<td></td>
<td>0.001272</td>
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</table>

<table>
<thead>
<tr>
<th>SPOT SIZE &amp; FOCUS SHIFT: UNITS mm</th>
</tr>
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<tbody>
<tr>
<td>WAVELENGTHS (microns)</td>
</tr>
<tr>
<td>W1: 0.852</td>
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Chip to chip interconnection
SPOT DIAGRAM ANALYSIS
SPARCL Prototype System Laboratory Setup

- Power supplies
- Monitor
- Monitoring camera
- Power meters
- SPARCL Boards & baseplate
- Oscilloscope
- Host computer
SPARCL Baseplate Layout

- Beam splitter
- Diffractive Grating
  (Spot array generator)
- Polarizers
- Risley prism pair
- On-site monochomater
- SPARCL boards
- Laser Beam
## Optical Source Collimation

<table>
<thead>
<tr>
<th>Laser Diode 1</th>
<th>Divergent Beam</th>
<th>Collimated Beam</th>
<th>Convergent Beam</th>
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</thead>
<tbody>
<tr>
<td><img src="image1.jpg" alt="Image" /></td>
<td><img src="image2.jpg" alt="Image" /></td>
<td><img src="image3.jpg" alt="Image" /></td>
<td></td>
</tr>
<tr>
<td>Laser Diode 2</td>
<td>Divergent Beam</td>
<td>Collimated Beam</td>
<td>Convergent Beam</td>
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<tr>
<td><img src="image4.jpg" alt="Image" /></td>
<td><img src="image5.jpg" alt="Image" /></td>
<td><img src="image6.jpg" alt="Image" /></td>
<td></td>
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</tbody>
</table>
Experimental Results -
Diffraction Spot Arrays Generated from Microlens Arrays

- Microlens array 1
- Microlens array 2
- Microlens array 3
- Microlens array 6
- Microlens array 8
- Microlens array 9
Characterization of CMOS/MQW devices
- Modulator reflectivity measurement setup

Measurement Reliability:
- Wavelength stability
  - Stabilized $\lambda$ through grating assisted external cavity of laser diode assembly
  - In-situ wavelength monitor with 0.2 nm monochromater
- Spot alignment
  - Coarse adjustment by visual alignment
  - Fine adjustment by maximizing photo-current

- Collimation
- Aberration
- Repeatability
Measurement of modulator reflectivities across 5x10 SPARCL chip

Reflectivity (reflected/incident optical power)

Reversed bias voltage (2 - 12 volts)

• The reflectivity of MQW diode varies in a certain range from diode to diode
Optimization of modulator bias voltage for best contrast ratios for $Q_1/Q_2$ and $Q_2/Q_1$.

- Photon absorption rate of MQW varies from device to device.

- Contrast Ratio $Q_1/Q_2$ (logic “0”) = $\frac{\text{reflected power of } Q_1 \text{ with bias } V_{\text{mod}-}}{\text{reflected power of } Q_2 \text{ with bias } V_{\text{mod}+}}$

- Contrast Ratio $Q_2/Q_1$ (logic “1”) = $\frac{\text{reflected power of } Q_2 \text{ with bias } V_{\text{mod}-}}{\text{reflected power of } Q_1 \text{ with bias } V_{\text{mod}+}}$

- $V_{\text{mod}+} - V_{\text{mod}-} = V_{\text{dd}}$

- CR of $Q_1/Q_2$ is optimized at $V_{\text{mod}+} = 11.25 \text{ V}$
- CR of $Q_2/Q_1$ is optimized at $V_{\text{mod}+} = 10.75 \text{ V}$

Optimize CR at $V_{\text{mod}+} = 11 \text{ V}, \quad V_{\text{mod}-} = 6 \text{ V}$
Contrast ratio profiles for Q₁/Q₂ and Q₂/Q₁ over entire 5 ⅞ 10 array

CR profile of Q₁/Q₂

CR profile of Q₂/Q₁

contrast ratio Q₁/Q₂, mean = 1.96

contrast ratio Q₂/Q₁, mean = 2.13
Operation of CMOS/MQW SPARCL Chip

- Eye diagram from single MQW modulator

- **Power budget**
  - Static power dissipation ~400 mW due to 50 transimpedance receivers
  - Dynamic power dissipation at 20 MHz ~100 mW
  - Total chip power dissipation about 500 mW

- Optical switching power of single detector is about 1.5 µW per MQW diode

(time scale 1.5 µs/div)
Smart Pixel Array Network Interface (SAPIENT)

- Ring connected 3 nodes network system
- 3x3 packet size with 2 bits address header and 7 bits payload
- Embedded with smart add/drop multiplexing capability
Schematic Design of Single SAPIENT Pixel

- Two data inputs: DET(optical) and ELE_IN(electrical)
- Three control signals from control unit - ADD_CELL, DROP_CELL and match_loadUnload
- Two data outputs: LED(optical) and ELE_OUT(electrical)
Schematic Design of On-chip Control Unit

- match=1 if DET=node_address
- ADD_CELL=1, if (i) SEND_CELL=1 and
  (ii) DROP_CELL=1 or DET="00"
- match_load_unload=1 if match=1 or load=1 or unload=1
Physical Layout of Single SAPIENT Pixel

OPFET (detector)

LED (transmitter)

150 µm

380 µm
Timing Diagram of SAPIENT Chip

- Embedded Smart Add/Drop Multiplexing
Floor Plan of SAPIENT Chip

Legend:
- detector
- led

Smart Pixel Array pads(14):
- clock, clear
- 2 control lines (SEND, Load_Unload)
- 2 address bits
- 6 ele_ins/outs
- 2 ACKs

Power Pads(6):
- Vdd
- GND
- Vbias_bg(backgate)
- Vled_p
- Vdd_hc (iboost)
- GND_hc (iboost)

Ring Oscillator pads(3):
- 1 Select
- 1 Input
- 1 Outputs
Physical Layout of SAPIENT Chip

- Process: 0.8 μm Vitesse HGaAs3 standard process through MOSIS
- LED emission spectrum: peak at 873 nm
- LED radiated power: ~4.5μW/mA/LED (or 15mW at 2V bias voltage)
- OPFET detector sensitivity: 0.4mA at 1W/cm² light intensity
- Power consumption: ~600mW at 200MHz
• optical parallel packets are transmitted asynchronously around the ring
• network clock rate in each node is equal to half of the chip clock rate
• for minimum latency, nodes are “translucent” when not transmitting
Translucence Smart Pixel Array (TRANSPAR)

- translucent mode - combinational logic only (no clocked circuits)
- detects, amplifies and retransmits (no retiming or filtering)
- not physically transparent (blocks low level noise on the network)

- low latency due to asynchronous operation (1ns/node + time of flight)

Equivalent electrical representation of a single network channel:

```
node 1
1 ns
receive

node 2
1 ns
translucent

node 3
1 ns
send

node 4
1 ns
translucent

node 5
1 ns

node 6
1 ns
```
Architecture of the Smart Pixel Processing Element

- optical network interface
  - dual-rail one-bit Rx and Tx
  - 2:1 mux opaque/ transparent
  - 8 bit FIFO - interface for asynchronous operation

- data processing
  - bit-slice ALU operating on variable number of bits
  - 32-bit SRAM
  - three registers (RA, RB, RC)
  - neighborhood mesh routing
  - enable bit stored in RC
  - fully controlled by the FSM, but can be accessed from outside the chip for debugging
Carrier Sense Multiple Access with Collision Detection (CSMA/CD)

Protocol Description:

- **Smart local carrier sense and collision detection without global handshaking**
- **Network Topology**: assume ring connected 6 nodes network with node addresses from “001” to “110”.
- Source and destination address “000” are reserved as empty address.
- Source address “111” is reserved as collision address.
- Destination address “111” is reserved for broadcast.
- **Types of Collision**:
  - **Type I**: non-trivial address change detected. (e.g. address change from 000 to 001 is a trivial change and is NOT considered a collision)
  - **Type II**: the node is a sender and receives packet from other nodes. The sender uses 111 as source address when type II collision occurs.
- **Smart identification of collision**
  - if the node is a sender or a receiver, reset CD signal by host computer
  - if the node is not sender nor receiver, reset CD signal automatically
- **BLOCK v.s. SEND**: After sending the packet, the sender keeps block the network and padding with 0’s until CS becomes low to prevent ghost packet flying on network forever.
Carrier Sense Multiple Access (CSMA)

Assume:
- Propagation delay: 5 ns/node
- Traffic: 1 -> 3
- Packet length: 8 frames

Bit Rate:
200 Mbps (or 5 ns/bit)

: sender is opaque but sending out nothing - zeros and no clock
Simulation of CSMA/CD Protocol

CSMA/CD - Successful transmission (Simulation at node 1)
Simulation of CSMA/CD Protocol

CSMA/CD - Collision in Packet (Simulation at node 1)
Schematic of CSMA/CD Design

Detected Sender Address (3 bits)

Optical Clock

Source Address (3 bits)

Carrier Sense

Collision Detection

Transmitter

Detected Sender Address

Optical Clock

Source Address

Collision Detection

Transmitter

Detected Sender Address

Optical Clock

Source Address

Collision Detection

Transmitter

Detected Sender Address

Optical Clock

Source Address

Collision Detection

Transmitter
Bell Labs OE/VLSI: MQWs flip-chipped to HP 0.5 CMOS
28,000 transistors (10mW @ 3.3V static, 200mW at 200 MHz on-chip clock)
TRANSPAR OE/VLSI Layout

- Bell Labs OE/VLSI: MQWs flip-chip bonded to HP 0.5 CMOS
- Smart pixel designs
  - 4 x 8 mesh-connected PE’s
  - 3-bit destination address and 3-bit source address
  - optical clock pixel

- Control/interface/clock
  - Finite State Machine
  - CSMA/CD protocol
  - Internal clock (up to 350 MHz)
    - external clock
    - VCO with PLL (ext clk x 16)
- 28K transistors (4 mA @ 3.3V)
AT&T Bell Lab System5 Switching Fabric

- 1995 demonstration system5: 32 node switching network
- 1996 demonstration system6: 256 node ATM switch
  - 155 Mb/s
  - 4352 optical ports per chip

(S. J. Hinterlong, et. al., 1996 IEEE summer topical meeting on smart pixels, pg 47)
Optical Backplane (U of Colorado, McGill)

- Optical backplane for interconnecting PCBs
  - PCBs inject data to backplane at rates (< 10 Gb/s)
  - optical backplane data rate between PCBs (> 100 Gb/s)
- Possibility of adding intelligence to backplane

Photonic Random Access Memory Architecture

256M SDRAM
- 1M words with 64 bits/word
- Electrical addressing
- Parallel optical data transfer
- 16x16 optical receiver array for data input
- 16x16 optical transmitter array for data output
- 10 row addresses, 10 column addresses for 1M words access

1Mbits memory block with 1 bit optical I/Os
Photonic RAM Building Block

- 1 Mbits random memory access with 1 bit optical data I/O
Summary

1. Presented a Free Space Digital Optics (FSDO) system using CMOS/MQW smart pixel arrays for high capacity parallel pipeline SIMD data processing
2. Architectural design of SPARCL CMOS/MQW chip for cellular pipeline computing
3. Construction and testing of the prototype optoelectronic system and characterization of CMOS/MQW devices
4. Demonstration of SPARCL system for digital video motion estimation
5. Presented Smart Pixel Array technology for network add/drop multiplexing (SAPIENT chip)
6. Present Smart Pixel Array technology for ring connected gigabit Ethernet application (TRANSPAR chip)