通訊系統晶片實驗室 (Communication System on Chip Laboratory)

The lab is dedicated to the R&D of system-on-chip (SoC) approaches for digital communication systems. It covers system and VLSI design for all kinds of digital communication technologies, including communication SoC platform development, hardware/software partition of baseband communication, VLSI for signal processing, communication modulation, channel coding, error correction, and communication synchronization techniques.
Research Interests

(1) Communication SOC Platform
   - AMBA 2.0 or AXI based SOC platform for communication systems

(2) Communication Receiver
   - Spread spectrum techniques in baseband communication IC design including DS, FH, CCK, OFDM, and WCDMA
   - Channel coding/decoding, error correction techniques in baseband communication transceiver design.
   - Communication synchronization techniques used in baseband communication IC design, including timing estimation, frequency synchronization, channel estimation

(3) Communication Transmitter
   - Predistortion of PA non-linearity
   - PAPR reduction for OFDM Transmitters

(4) Optical signal processing
   - Switching Fabric for Optical Fiber Communication
Past Experience - SIMD Image Processing IC

- Design and Layout of Smart Pixel ARray Cellular Logic (SPARCL) Chip for video motion estimation
- 5 x 10 CMOS/MQW smart pixel SIMD array processing
- Standard 0.8 µm HP CMOS foundry process via MOSIS
- MQW foundry service from Bell Labs/Lucent Technologies

![Diagram of Single Smart Pixel](image)
Past Experience - IC testing and Demo

- SPARCL Boards & baseplate
- Monitor
- Power supplies
- Monitoring camera
- Power meters
- Host computer
- Oscilloscope
Past Experience - networking IC

- Bell Labs OE/VLSI: MQWs flip-chip bonded to HP 0.5 CMOS
- Smart pixel designs
  - 4 x 8 mesh-connected PE’s
  - 3-bit destination address and 3-bit source address
  - optical clock pixel
  - Finite State Machine
- Control/ interface/ clock
  - CSMA/CD protocol
  - Internal clock (up to 350 MHz)
    - external clock
    - VCO with PLL (ext clk x 16)
- 28K transistors (4 mA @ 3.3V)

High capacity ring connected Ethernet with CDMA/CD protocol
Past Experience: Sun Microsystems

- VLSI Design and Verification Engineer of Sun Microsystems, Sunnyvale, CA, in many successful products.
  - UltraSPARC III-Al microprocessor
    (for low/mid-range server, 900MHz, 0.18um, Al.),
  - UltraSPARC III-Cu (for high end server, 1.2GHz, 0.18um, Cu.),
  - UltraSPARC IV-Cu (for high end server, 1.8 - 2.0 GHz, 0.13um, Cu.)
What is doing now- (1) Comm. SoC platform

- AMBA 2.0 or AXI Centric SOC Platform
- Focused on AMBA enabling IP’s-
  - Arbiter, Decoder, TIC and APB Bridge
AMBA based communication SoC platform
What is doing now- (2) Comm Receiver

- Timing Synchronization
- Freq Synchronization
- Channel Coding
- OFDM
- Broadband Wireless
What is doing now- (3) Comm Transmitter

- Predistortion for PA (power amplifier) non-linearity
- Optimization of PAPR (Peak-to-Average Power Ratio) reduction for OFDM waveform in time domain given saturation characteristics of PA
- The trend is to use digital design as much as possible. DSP is changing the game of RF circuit design.
To Prospective Graduate Students

If you think you are highly motivated, self-disciplined, initiative, smart, and energetic, come see me.

For students who show these qualities, I will be a very supportive advisor, working closely with them to develop their knowledge and research potential and help them launch productive careers in academic or industrial research.

Students should have a strong background in the fundamentals of theories and engineering. While most of the work in my lab is systems-oriented and involves a significant amount of experimental work, I believe strongly that the best systems work must be informed by a deep understanding of fundamental principles and I am most interested in students with the ability to use their knowledge creatively to conceive and design innovative new systems.
Selected Journal Publications