The Purpose
1. To get familiar with front end tools (verilog compiler, Debussy, and Synopsys Design Compiler) for digital logic synthesis.
2. To get familiar with RTL coding with verilog.
3. With this example you will gain some experience about implement a simple correlator for digital communication.

The Assignment
1. Consider packet detection using binary hypothesis:
   \[ H_0: \text{packet not present} \]
   \[ H_1: \text{packet present} \]
   The actual test is usually of the form that tests whether a decision variable \( m_n \) exceeds a predefined threshold \( T_h \)
   \[ H_0: m_n < T_h \ (\text{packet not present}) \]
   \[ H_1: m_n \geq T_h \ (\text{packet present}) \]
   Let the decision variable \( m_n \) change in energy level, i.e. the auto-correlation, as defined in the following equation
   \[ m_n = \sum_{k=0}^{L-1} r_{n-k}^* r_{n-k} = \sum_{k=0}^{L-1} |r_{n-k}|^2 \]
   You are supposed to design packet detection for a receiver using this method. You may specify your own threshold value.
   (1) Please draw a block diagram of the design. (20%)
   (2) Let \( L = 4 \) and the I channel and Q channel values of each input signal \( r_n \) are represented by 4 bit word length. Please implement packet detection function in Verilog RTL design. Please turn in your verilog file. (20%)
   (3) Please synthesis your design with Synopsys at clock rate of 200MHz and generate your netlist. (20%)
   (4) Please find the static timing of your design and turn in your timing report. (20%)
   (5) Let the received signal \( r_n \) for \( n = 0, 1, 2, ..., 19 \) be
   \( 0,0,0,0,0,0,1+j, 1-j, -1+j, -1-j, 1+j, 1-j, -1+j, -1-j, 0,0,0,0,0 \)
   Please find and verify the output in Debussy. (20%)