Key to SOC Success

- SOC – System On Chip
- SOC Trends
- Design and verification methodology
System On Chip

System On Chip – Consist of two parts
- Hardware: System architecture & chip architecture
- Software: Device driver & operating system

Chip manufacture/Design House need to provide a Total Solution for your customers.
- Reference design/complete product
- Application support
SOC Trends

Three Trends of SOC
(According to Dave Reed of Cadence Design)
- Application Convergence
- Consumerization of the electronics industry
- Exponential growth of available transistor
SOC Trends

- Application Convergence
  - Set top boxes
    - Decode cable signals
    - Internet access
    - Digital Video Recorder
  - Cell Phone
    - Traditional cell phone
    - MP3 player
    - Digital Camera
    - PDA
SOC Trends

- Consumerization of the electronics industry
  - Design cycle times are now dictated by the consumer.
    - One year the most
  - Majority of the functions are pushed to chip.
    - Lower cost
    - Lower Power
  - The ability to rapidly generate variants of the SOCs will be required to meet the consumer time frame and quench the thirst for differentiation.
SOC Trends

- Exponential growth of available transistor
  - 100 + million transistors can be made on a single die
  - The cost of the transistor is approaching free
    - $10^{-5}$ cents / transistors (US dollar)
SOC Trends

Challenge for the chip design house
- Chip company need to acquire system knowledge, both hardware and software.
- Need for increasing the productivity of design activity by adopt effective design reuse methodology.
- Harder to test millions of transistor on a single die. Design for Test is critical for the success of products.
System Knowledge

- Hardware / Software tradeoff
  - Application Driven
  - Cost Driven
- Software Platform (require operating system?)
  - Linux Operating System
  - Device driver
- Hardware Performance requirement
  - IO/Data Bus Throughput
  - CPU/DSP processing power
Design for Reuse (In House IP)

- Integration-Driven Reuse
  - Focus on the needs of the IP integrator – the SOC designers.
  - Internal Bus Architecture
    - Pipeline/Non-Pipeline
    - Central arbitration/distributed arbitration
  - DMA architecture
    - Software model / descriptor definition
    - Memory to Memory / Device to Memory
Design for Reuse (In House IP)

- Integration-Driven Reuse (cont)
  - System Register File
    - Central / distributed
    - Address mapping
  - Debug Logic
    - Capture bus trace
    - Direct control of internal bus
    - Direct control of internal register
IP Availability for Licensing

Typical IP available for purchase
- CPU: ARC, ARM, Tensilica and MIPS
- Bus Interface: PCI and PCIX
- Serial Interface: I2C, IrDA, UART and USB
- LAN: Ethernet 10/100/1000 MAC, HDLC, SONET Framer, Transceiver and Framer.
- Memory Compiler: Artisan, Dolphin Tech and Virage
Cell Based Design Flow

- RTL
  - Synthesis
    - Gate Netlist
      - Extraction & Delay Calculation
        - RC
        - P & R
          - Static Timing Analysis
            - GDS
              - Tapeout
CAD Tools

- Logic Simulation
  - VCS (Synopsys)
  - NC Verilog (Cadence)
- Synthesis
  - Design Compiler (Synopsys)
  - Ambit (Cadence)
- Static Timing Analysis
  - Primetime (Synopsys)
- P&R
  - Apollo-II (Avant)
  - Silicon Ensemble (Cadence)
Verification Environment

- Verification occupy higher percentage of total effort.
- Random Test Generation is a must
  - Micro Architecture verification
  - System level verification
- Micro Architecture verification environment need to be reusable in the system level verification
- Transactor development
Design For Testability

- To ensure high quality of production parts
  - Functional pattern can no longer achieve the high coverage in the complex SOC design.
- Build In Self Test (BIST)
  - Embedded memory
- Scan Insertion
  - Random logic
  - Stuck-fault model
  - Increase controllability and observeability
Design For Testability

- Timing test
  - Functional tests
  - Using scan path

- Other games you can play
  - Combine Primary Inputs and Exclusive-Or Primary Output
  - Changing scan clock frequency to test timing path
You need software to help you manage your complex design data base.

Revision Control (for text file)
  - CVS
  - RCS

Bug Tracking
  - GNATS
Business Model

Division of work

- System house: system software development, board design and sales channel
- SOC: Micro architecture, specialty IP development, IP integration and basic software platform development.
- Design service: providing IP, backend, foundry and packaging support
Conclusion

- High entry barrier, but high reward
- First design is always difficult, but it will get easier.
- System knowledge
- This is not a rocket science. Experience is everything.
  - Retain experienced designers to ensure long term success.